The official voice of the Air Force Research Laboratory
news@afrl
Roundups
January 2004

Information Directorate awards $1.1M to Boeing

by Fran Crumb, Information Directorate

ROME, N.Y. — The Air Force Research Laboratory's Information Directorate has awarded a $1,195,010 contract to The Boeing Co. of Seattle, Wash.

The six-month agreement, "Clockless Logic Analysis, Synthesis and Systems (CLASS)," is funded by the Defense Advanced Research Projects Agency (DARPA) of Arlington, Va., under its Design Tools for Integrated Asynchronous Electronic Circuits program.

The emphasis of the CLASS program is on the development of asynchronous digital logic integrated circuit design techniques that overcome issues with the dominant synchronous (clocked) design methodology.

Under this program, an evaluation and design environment infrastructure will be developed and used to demonstrate advantages of asynchronous logic implementations to achieve drastically reduced design effort, improved energy utilization, reduced electromagnetic interference, and increased robustness (voltage and process variation) compared to corresponding clocked designs. The ultimate purpose of the CLASS program is to enable the rapid design of highly complex, asynchronous System-on-a-Chip devices that would not be practical with the traditional, full-custom, synchronous circuit design approach, especially in the coming sub-100nm domain.

The Boeing award is for the first phase of a three-phase research program. Subsequent awards could increase the value of the contract to more than $10 million.

Clockless chips have already been demonstrated for high-performance applications with significantly reduced power consumption. Despite these prototype demonstrations, asynchronous architectures have not found wide acceptance in the electronics industry due to the lack of an infrastructure to design, test and fabricate asynchronous chips in a reliable, efficient and economical way.

The lack of commercially supported CAD tools for asynchronous design has been a significant barrier in developing clockless chips and DARPA is pursuing the feasibility of developing a new generation of those tools to spur development of the technology. @